CS-03-023

April 30, 2004

To: Commissioner for Patents
P.O.Box 1450
Alexandria, VA 22313-1450

Fr: George O. Saile, Reg. No. 19,572
28 Davis Avenue
Poughkeepsie, N.Y. 12603

Subject: Serial No. 10/776,793 02/11/04

Indrajit Manna et al.

TRIGGERED SILICON CONTROLLED RECTIFIER FOR RF ESD PROTECTION

INFORMATION DISCLOSURE STATEMENT

Enclosed is Form PTO-1449, Information Disclosure Citation In An Application.

The following Patents and/or Publications are submitted to comply with the duty of disclosure under CFR 1.97-1.99 and 37 CFR 1.56.

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on May 4, 2004.

Stephen B. Ackerman, Reg.# 37761

Signature/Date 5/4/04

U.S. Patent Application Publication US 2003/0016479 A1 to Song, "Electrostatic Discharge (ESD) Protection Circuit of Silicon-Controlled Rectifier (SCR) Structure Operable at a Low Trigger Voltage," describes an ESD protection circuit having silicon-controlled rectifier structure that includes a PNP transistor and an NPN transistor.

U.S. Patent 6,605,493 to Yu, "Silicon Controlled Rectifier ESD Structures with Trench Isolation," teaches about an SCR ESD protection device used with shallow trench isolation structures.

U.S. Patent 6,580,184 to Song, "Electrostatic Discharge (ESD) Protection Circuit of Silicon-Controlled Rectifier (SCR) Structure Operable at a Low Trigger Voltage," illustrates an ESD protection circuit having a silicon-controlled rectifier structure.

U.S. Patent 6,534,834 to Ashton et al., "Polysilicon Bounded Snapback Device," teaches about a snapback device that functions as a semiconductor protection circuit to prevent damage to integrated circuits resulting from events such as electrostatic discharage.

U.S. Patent 6,610,262 to Peng et al., "Depletion Mode SCR for Low Capacitance ESD Input Protection," describes an ESD semiconductor protection with reduced input capacitance.

U.S. Patent 5,453,384 to Chatterjee, "Method of Making a Silicon Controlled Rectifier Device for Electrostatic Discharge Protection," describes a silicon controlled rectifier structure that is provided for electrostatic discharge protection.

U.S. Patent 5,159,518 to Roy, "Input Protection Circuit for CMOS Devices," details an input protection circuit that protects MOS semiconductor circuits from electrostatic discharge voltages and from developing circuit latchup.

U.S. Patent 5,629,544 to Voldman et al., "Semiconductor Diode with Silicide Films and Trench Isolation," discusses a structure for improving device characteristics of protection diodes on chips having trench isolation and silicide contacts.

Voldman et al., "Electrostatic Discharge (ESD) Protection in Silicon-on-Insulator (SOI) CMOS Technology with Aluminum and Copper Interconnects in Advanced Microprocessor Semiconductor Chips," EOS/ESD Symposium 99-105, pp. 2A.6.1 to 2A.6.11, discusses the electrostatic discharge (ESD) robustness of silicon-on-insulator (SOI) high-pin-count high-performance semiconductor chips.

Voldman et al., "Semiconductor Process and Structural Optimization of Shallow Trench Isolation-Defined and Polysilicon-Bound Source/Drain Diodes for ESD Networks," EOS/ESD Symposium 98-151, pp. 3A.1.1 to 3A.1.10, discusses the impact of MOSFET source/drain junction scaling on ESD robustness of shallow trench isolation (STI)-defined diode structures, ESD robustness improvements to STI-bound p+ diodes using germanium preamorphization and deep B11 implants, and polysilicon-bordered ESD networks.

Sharma et al., "An ESD Protection Scheme for Deep Sub-micron ULSI Circuits," 1995 Symposium on VLSI Technology Digest of Technical Papers, pp. 85-86, describes a scheme for on-chip protection of sub-micron ULSI circuits against ESD stress using low voltage zener-triggered SCR, and a zener-triggered thin gate oxide MOSFET.

Sincerely,

Stephen B. Ackerman,
Reg. No. 37761

Form PTO-1449

INFORMATION DISCLOSURE CITATION IN AN APPLICATION

(Use several sheets if necessary)

OIPE JC33 MAY 0 6 2004 PATENT & TRADEMARK OFFICE

Docket Number (Optional)	Application Number
CS-03-023	10/776,793
Applicant: Indrajit Manna et al.	
Filing Date: 02/11/04	Group Art Unit:

U. S. PATENT DOCUMENTS

Examiner Initial	Document Number	Date	Name	Class	Subclass	Filing Date if Appropriate
	6610262	8/26/03	Peng et al.	423	197	3/4/02
	6605493	8/12/03	Yu	438	135	8/29/01
	6580184	6/17/03	Song	307	112	5/16/02
	6534834	3/18/03	Ashton et al.	257	355	12/19/01
	5159518	10/27/92	Roy	361	56	1/17/90
	5629544	5/13/97	Voldman et al.	257	355	4/25/95
	5453384	9/26/95	Chatterjee	437	6	3/25/94

FOREIGN PATENT DOCUMENTS

Examiner Initial	Document Number	Date	Country	Class	Subclass	Translation YES	Translation NO

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

Examiner Initial	
	US Patent App. Pub. US 2003/0016479 A1 to Song, Pub. Date 1/23/03, Filed 5/16/02, US Cl. 361/56.
	S. Voldman et al., "Electrostatic Discharge (ESD) Protection in Silicon-on-Insulator (SOI) CMOS Technology with Aluminum and Copper Interconnects in Advanced Microprocessor Semiconductor Chips", EOS/ESD Symposium 99-105, 2A.6.1 to 2A.6.11.

EXAMINER	DATE CONSIDERED

EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP § 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to the applicant.

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FOREIGN PATENT DOCUMENTS

	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	Translation YES	Translation NO

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

–	S. Voldman et al., "Semiconductor Process and Structural Optimization of Shallow Trench Isolation-Defined and Polysilicon-Bound Source/Drain Diodes for ESD Networks", EOS/ESD Symposium 98-151, 3A.1.1 to 3A.1.10.
–	Umesh Shama et al., "An ESD Protection Scheme for Deep Submicron ULSI Circuits", 1995 Symp. on VLSI Tech. Digest of Tech. Papers, pp. 85-86.

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